RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College under University of Calcutta)

B.A./B.SC. FIRST SEMESTER EXAMINATION, DECEMBER 2011

FIRST YEAR

Date : 21/12/2011 **ELECTRONICS (General)**

Time : 11am – 1pm Paper : I Full Marks : 50

Answer **any five** out of the following questions

1. a) Prove that the NAND gate is a Universally complete logic gate.
   b) Design an EX-OR gate using minimum number of NAND gates. 5+5

2. a) What is the rule to add two BCD numbers for getting the sum correct in BCD? Using the rule add the numbers 799 and 689 using BCD notation.
   b) Minimise the following function $F(A,B,C,D) = \sum m(0,2,8,10,13,15) + \sum d(6,11,14)$. (3+2)+5

3. a) Compare SOP and POS forms of Boolean functions.
   b) Design a full adder circuit with necessary logic gates. 5+5

4. a) Show that using 2-to-1 MUX one can realise all the three basic gates.
   b) Realise a function $F(A,B,C) = AB + BC + CA$ using one 4-to-1 MUX and other necessary basic gates. 6+4

5. a) What is the advantage of JK flip flop? What is its disadvantage and briefly discuss how you can overcome it.
   b) Briefly describe the function of a T-flip-flop. (2+2+3)+3

6. a) What do you mean by synchronous and asynchronous counters?
   b) Draw the circuit and explain the operation of a MOD-7 asynchronous counter. (2+2)+6

7. a) Design a 2-to-4 Decoder using NAND gates only.
   b) Explain a bi-directional shift register. 6+4

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